EFFICIENT POWER CONTROL OF A POWER AMPLIFIER
BY PERIPHERY SWITCHING

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RELATED APPLICATIONS

[0001]   The present invention is a continuation-in-part of
Provisional U.S. Patent Application Serial No. 60/412,342,
"Efficient Power Control by Periphery Switching", by Thomas
R. Apel, which was filed on September 20, 2002.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002]   The present invention relates to a method and
structure for improving the efficiency and linearity of a
power amplifier (PA). More specifically, the present
invention relates to a method and structure for turning off
a subset of the transistors in a power amplifier during low
power operation.

Related Art

[0003]   Linear power amplifiers are often operated in
class AB mode. Operation in class AB mode provides for
reduced power supply current to the power amplifier as the
power of the input signal is reduced. The power supply
current can be reduced until a minimum quiescent current is
reached. The direct current (DC) power to radio frequency
(RF) power efficiency degrades as the power of the input
signal is reduced. Prior art linear power amplifiers
provide some improvement in low power efficiency by stepping
the quiescent current to a lower level for low power
operation. However, the linearity of the power amplifier is
degraded at very low quiescent current levels.

[0004]   Fig. 1 is a circuit diagram illustrating a conventional power amplifier 100, which includes amplifier stages 101-102 and associated bias circuits 111-112. Each of amplifier stages 101-102 includes a parallel-connected set of NPN bipolar transistors 103-104, respectively. Ballast resistors 105-106 are connected to the bases of transistor sets 103-104. In general, the bases of transistor sets 103-104 are configured to receive a radio frequency input signal (e.g., RF_{IN}). The emitters of transistor sets 103-104 are coupled to ground, and the collectors of transistors sets 103-104 are configured to provide an RF output signal (e.g., RF_{OUT}) to an output terminal of the associated amplifier stage.

[0005]   When the input signal RF_{IN} is controlled to be a high power signal (i.e., during high-power operation), a HI/LO control signal is activated to a first logic state. In response, bias voltage control circuits 111-112 provide relatively high bias voltages V_{BIAS1}-V_{BIAS2}. As a result, amplifier stages 101-102 operate in a linear manner in response to the RF_{IN} signal. Conversely, when the input signal RF_{IN} is controlled to be a low power signal (i.e., during low-power operation), the HI/LO control signal is deactivated to a second logic state. In response, bias control circuits 111-112 provide relatively low bias voltages V_{BIAS1}-V_{BIAS2}. Under these conditions, amplifier stages 101-102 consume less power, but the linearity of power amplifier 100 is degraded under these conditions.

[0006]   It would therefore be desirable to have an alternative to the extremely low quiescent current operation (i.e., "current starved" operation) that results when the power supply current to the power amplifier is reduced as the power of the input signal is reduced.

SUMMARY

[0007] Accordingly, the present invention provides a power amplifier having a first amplifier output stage and a parallel-connected second amplifier output stage. The first amplifier output stage is enabled (i.e., fully biased) during both high power and low power operating modes. The second amplifier output stage is disabled during the low power operating mode, and enabled during the high power operating mode. Because neither the first nor second amplifier output stage is operated in a low quiescent current state, the linearity of the power amplifier is maintained for both high power and low power operating modes.

[0008] In a particular embodiment, one or more additional amplifier output stages can be connected in parallel with the first and second amplifier output stages, thereby enabling intermediate power operating modes.

[0009] The present invention will be more fully understood in view of the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Fig. 1 is a circuit diagram of a conventional power amplifier.

[0011] Fig. 2 is a circuit diagram of a power amplifier in accordance with one embodiment of the present invention.

[0012] Fig. 3 is a block diagram of an amplifier input stage and an input stage bias circuit of the power amplifier of Fig. 2, in accordance with one embodiment of the present invention.

[0013] Fig. 4 is a circuit diagram of the input stage bias circuit, an input cell, and impedance matching networks

in accordance with one embodiment of the present invention.

[0014]   Fig. 5 is a block diagram of amplifier output stages, bias circuits and a step control circuit of the power amplifier of Fig. 2, in accordance with one embodiment of the present invention.

[0015]   Fig. 6 is a circuit diagram of an output cell, a bias circuit and a step control circuit, in accordance with one embodiment of the present invention.

[0016]   Fig. 7 is a circuit diagram of an output cell and a bias circuit, in accordance with one embodiment of the present invention.

[0017]   Fig. 8 is a graph illustrating RF input power versus RF output power for the power amplifier of Fig. 2 in a high power mode and a low power mode.

[0018]   Fig. 9 is a graph illustrating RF input power versus collector current for the power amplifier of Fig. 2 in a high power mode and a low power mode.

[0019]   Fig. 10 is a block diagram of a power amplifier having three output stages, in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0020]   Fig. 2 is a circuit diagram of a power amplifier 200 in accordance with one embodiment of the present invention. Power amplifier 200 includes amplifier input stage 201, input stage bias circuit 211, amplifier output stages 221-222, output stage bias circuits 231-232, and step control circuit 250. In general, bias circuits 211, 231 and 232 cause DC bias voltages to be applied the bases of RF transistors present in input stage 201, output stage 221 and output stage 222, respectively. A radio frequency (RF) signal RF_{IN} is applied to input stage 201. In response,

input stage 201 provides an intermediate level RF signal RF_{INT} to output stages 221 and 222.

[0021]   If power amplifier 200 is operating in a high power mode, step control circuit 250 enables output stage 222 (via the BIAS_CTRL signal). In this case, both of output stages 221 and 222 provide an RF output signal RF_{OUT} in response to the intermediate level RF signal RF_{INT}.

[0022]   If power amplifier is operating in a low power mode, step control circuit 250 disables output stage 222. In this case, only output stage 221 provides the output signal RF_{OUT} in response to the intermediate RF signal RF_{INT}.

[0023]   Advantageously, the RF transistors in output stage 221 always operate at a normal fully biased state. Similarly, the RF transistors in output stage 222 either operate at a normal fully biased state, or are disabled. In the low power state, the overall quiescent current is reduced by the ratio of the number of RF transistors in output stage 222 to the number of RF transistors in output stage 221. The advantage with this approach is in linearity. In all power states (high or low), the RF transistors are adequately biased for linear performance. In the described embodiment, the input and output interfaces to all RF transistor cells are all maintained. Thus, impedance matching and loading are unchanged, regardless of the power state.

[0024]   Power amplifier 200 will now be described in more detail. Fig. 3 is a block diagram of amplifier input stage 201 and input stage bias circuit 211, in accordance with one embodiment of the present invention. Amplifier input stage 201 includes input cells 301-302 and impedance matching networks 311-312. Impedance matching network 311 provides a filtered and matched RF signal RF_{INF} to input cells 301-302

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in response to the input RF signal RF_{IN}. Input cells 301-302, which are connected in a parallel configuration, provide amplified signals to impedance matching network 312. In response, impedance matching network 312 provides the intermediate RF signal RF_{INT}.

[0025] Fig. 4 is a circuit diagram illustrating bias circuit 211, input cell 301, and impedance matching circuits 311-312 in accordance with one embodiment of the present invention. Note that input cell 302 (not shown in Fig. 4) is identical to input cell 301. Impedance matching circuit 311 includes capacitors 401-402 and inductors 411-412. Impedance matching circuit 312 includes capacitor 403 and inductor 413. Bias circuit 211 includes capacitor 404, NPN bipolar transistors 421-424 and resistors 431-432. Input cell 301 includes capacitors 405-407, inductor 414, NPN bipolar transistors 425-428 and resistors 433-436. In general, the RF_{INF} signal is provided to the base of RF transistor 428. RF transistor 428 is biased by bias reference circuit 211 (which is common to both input cells 301 and 302), and distributed bias circuit 410 (which is specific to input stage 301, and includes capacitor 405, transistors 425-427 and resistors 433-435). Bias reference circuit 211 and distributed bias circuit 410 form a temperature adaptive bias circuit, which is described in more detail in commonly-owned, co-pending U.S. Patent Application Serial No. 10/421,679, which is hereby incorporated by reference. In general, bias circuit 211 and distributed bias circuit 410 provide a bias voltage on the base of RF transistor 428 in response to a first bias voltage V_{BIAS1}. When properly biased, RF transistor 428 provides a collector current, which when combined with a corresponding collector current in input cell 302, creates

the RF_{INT} signal.

[0026]   Fig. 5 is a block diagram of amplifier output stages 221-222, bias circuits 231-232 and step control circuit 250. Amplifier output stage 221 includes four output cells 501-504. As described in more detail below, output cells 501-504 are enabled during both low and high power operating modes. Amplifier output stage 222 includes twelve output cells 505-516. As described in more detail below, output cells 505-516 are enabled during the high power operating mode, and disabled during the low power operating mode. Output cells 501-516 are configured to receive the RF_{INT} signal in parallel, and provide the RF output signal, RF_{OUT}, in parallel.

[0027]   Fig. 6 is a circuit diagram of output cell 505, bias circuit 232 and step control circuit 250, in accordance with one embodiment of the present invention. Note that output cells 506-516 (not illustrated in Fig. 6) are identical to output cell 505. Bias circuit 232 includes capacitor 601, NPN bipolar transistors 621-624 and resistors 631-632. Output stage 505 includes capacitors 602-603, NPN bipolar transistors 625-628 and resistors 633-638. Step control circuit 250 includes NPN bipolar transistors 629-630 and resistors 639-640.

[0028]   In general, the RF_{INT} signal is provided to the base of RF transistor 628 via coupling capacitor 603. The base of RF transistor 628 is DC biased by bias circuit 232 (which is common to output cells 505-516), and distributed bias circuit 610 (which is specific to output cell 505). Bias circuit 232 and distributed bias circuit 610 form a temperature adaptive bias circuit, which is similar to the temperature adaptive bias circuit formed by bias circuit 211 and distributed bias circuit 410 (Fig. 4). In general, bias

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circuit 232 and distributed bias circuit 610 provide a bias voltage on the base of RF transistor 628 in response to a second bias voltage V_{BIAS2}. When step control circuit 250 allows output cell 505 to be properly biased, RF transistor 628 provides a collector current, which when combined with corresponding collector currents in output cells 501-504 and 506-516, creates the RF_{OUT} signal. Resistor 638 provides optional emitter biasing of RF transistor 628.

[0029] Step control circuit 250 includes NPN bipolar transistors 629-630 and resistors 639-640. When operating in the high power state, the V_{STEP} voltage has a logic high state, such that transistor 629 is turned on and transistor 630 is turned off. As a result, the BIAS_CTRL current is approximately equal to zero. Under these conditions, step control circuit 250 does not affect the operation of output cell 505 (or output cells 506-516). That is, bias circuits 232 and 610 operate to provide an appropriate DC bias voltage to the base of RF transistor 628, thereby enabling this transistor to contribute collector current to the RF_{OUT} signal.

[0030] When operating in the low power state, the V_{STEP} voltage has a logic low state, such that transistor 629 is turned off and transistor 630 is turned on. As a result, a significant BIAS_CTRL current is drawn from output cell 505 (through resistor 635) to ground. Under these conditions, transistor 626 turns off, thereby effectively disabling output cell 505 (and output cells 506-516). More specifically, when transistor 626 turns off, RF transistor 628 turns off due to insufficient DC bias on the base of this transistor.

[0031] Fig. 7 is a circuit diagram of output cell 501 and bias reference circuit 231, in accordance with one

embodiment of the present invention. Note that output cells 502-504 (not illustrated in Fig. 7) are identical to output cell 501. Bias reference circuit 231 includes capacitor 701, NPN bipolar transistors 721-724 and resistors 731-732. Output cell 501 includes capacitors 702-703, NPN bipolar transistors 725-728 and resistors 733-737.

[0032]   In general, the RF_{INT} signal is provided to the base of RF transistor 728 via coupling capacitor 703. The base of RF transistor 728 is DC biased by bias reference circuit 231 (which is common to low power mode output cells 501-504), and distributed bias circuit 710 (which is specific to output cell 501). Bias circuit 231 and distributed bias circuit 710 form a temperature adaptive bias circuit, which is similar to the temperature adaptive bias circuit formed by bias circuit 232 and distributed bias circuit 610 (Fig. 6). In general, bias circuit 231 and distributed bias circuit 710 provide a bias voltage on the base of RF transistor 728 in response to a second bias voltage V_{BIAS2}. When properly biased, RF transistor 728 provides a collector current, which when combined with corresponding collector currents in output cells 501-504 and 506-516, creates the RF_{OUT} signal. Resistor 737 provides optional emitter biasing of RF transistor 728. Notably, output cell 501 is not coupled to step control circuit 250. Thus, output cell 501 (and associated output cells 502-504) are enabled during both high and low power modes.

[0033]   Fig. 8 is a graph 800 illustrating the RF input power versus the RF output power of power amplifier 200 for the high power mode and the low power mode. Line 801 represents operation in the high power mode, wherein all of the output cells 501-516 are enabled. Line 802 represents the low power mode, wherein output cells 501-504 are enabled

and output cells 505-516 are disabled. Note that even though power amplifier 200 is operating at low power, the amplifier continues to operate with a high linearity.

[0034]   Fig. 9 is a graph 900 illustrating the RF input power versus the collector current of the RF transistors in output cells 501-516. Line 901 represents operation in the high power mode, wherein all of the output cells 501-516 are enabled. Line 902 represents the low power mode, wherein output cells 501-504 are enabled and output cells 505-516 are disabled. Fig. 9 illustrates the improvement in efficiency in the low power mode, because a reduction in current translates to a reduction in power (VxI).

[0035]   Although the present invention has been described in accordance with one output stage that is always enabled (output stage 221) and one output stage that is selectively enabled/disabled in view of the operating mode (output stage 222), it is understood that other configurations are possible. For example, in accordance with another embodiment of the present invention, output stage 221 can be enabled/disabled in a complementary manner with respect to output stage 222. Thus, during low power mode, output stage 221 is enabled and output stage 222 is disabled. Conversely, during high power mode, output stage 221 is disabled and output stage 222 is enabled. This embodiment could be implemented by providing a step control circuit (similar to step control circuit 250) for output stage 221.

[0036]   In another variation, a power amplifier can be created using more than two parallel output stages. Fig. 10 is a block diagram of a power amplifier 1000 having three parallel output stages, in accordance with one embodiment of the present invention. In addition to the above-described elements of power amplifier 200, power amplifier 1000

includes third amplifier output stage 223, bias control circuit 233 and step control circuit 251. Amplifier output stage 223, bias control circuit 233 and step control circuit 251 are similar to output stage 222, bias control circuit 232 and step control circuit 250, respectively. However, in the described embodiment, amplifier output stage 223 has more output stages than amplifier output stage 222. Step control circuit 251 operates in response to a second step control signal V_{STEP2}. Thus, step control circuit 251 operates independent of step control circuit 250. Power amplifier 100 advantageously allows for more than two power operating states. In the lowest power state, only amplifier output stage 221 is enabled. In a first power state, only amplifier output stages 221 and 222 are enabled. In a second power state, only amplifier output stages 221 and 223 are enabled. In a high power state, all amplifier output stages 221-223 are enabled. In an alternate embodiment, the functionality of step control circuits 250 and 251 can be combined in a single control circuit. The present embodiment can also be extended to more than three parallel amplifier output stages.

[0037]   The technique of the present invention can be used in different types of power amplifiers, including but not limited to, code division multiple access (CDMA) power amplifiers, wideband code division multiple access (WCDMA) power amplifiers, and enhanced data rates for GSM evolution (EDGE) power amplifiers.

[0038]   Although the invention has been described in connection with several embodiments, it is understood that this invention is not limited to the embodiments disclosed, but is capable of various modifications, which would be apparent to one of ordinary skill in the art. For example,

although amplifier input stage 201, and amplifier output stage 221 and amplifier output stage 222 have been described as having certain numbers of parallel RF transistors (i.e., 2, 4 and 12, respectively), it is understood that these amplifier stages can have other numbers of parallel RF transistors in other embodiments. Thus, the invention is limited only by the following claims.